In the Specification

Applicant presents replacement paragraphs below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please replace the paragraph commencing on page 13, line 31, through page 14, line 2 as follows:

The DAC 150 may receive a non-overlapping 3-phase clock, P1, P2, P3, shown in FIG. 6. The closed/open condition of the switches S3, S6, S9, and S12 is controlled by the P3 signal of the 3-phase clock. The P1 signal of the 3-phase clock controls the open/closed condition of the charge sharing switches [[S13,]] S14, S15, and S16. The P2 signal of the 3-phase clock controls the open/closed condition of the switch S17. The logical-OR of the P1 and P2 signals, P1+P2, controls the open/closed condition of the switch S13. That is, S13 closes when either P1 or P2 is in a logical high state.

Please replace the paragraph commencing on page 17, lines 11-26 as follows:

Referring now to FIG. 10, in another embodiment, the SC DAC 150 described with respect to FIGS. 7A-7C operates with a non-overlapping four-phase clock, e.g., the four-phase clock illustrated in FIG. 9 instead of the ~~three phase~~ three-phase clock of FIG. 6. On phase P3 of the ~~four phase~~ four-phase clock, the condition of the SC DAC 150 is the same as that described above with respect to FIG. 7A. On phase P4 of the ~~four phase~~ four-phase clock, the condition of the SC DAC 150 is the same as that described above with respect to FIG. 7B. On phase P1 of the ~~four phase~~ four-phase clock, the condition of the SC DAC 150 is the same as that described above with respect to FIG. 7C. FIG. 10 shows the state of the SC DAC 150 on phase P2 of the ~~four phase~~ four-phase clock. On phase P2 of the ~~four phase~~ four-phase clock, the charging switches S3, S6, S12 (FIG. 5) are in the open condition, ~~charge sharing~~ charge-sharing switches

S13, S15, S16 are in the open condition, and switch S14 and output switch [[S19]] S17 are in the closed condition, wherein C2 of the one-bit DAC delivers its charge to the output terminal 160. Thus, in such embodiment, two copies, each indicative of the sum of the values of the bits in the multi-bit digital input signal, are separately delivered to the output terminal. As described above, in this embodiment, they are delivered one after the other. However, in another embodiment, they may be delivered simultaneously.

In the Drawings

A Request for Approval of Proposed Drawing Corrections is enclosed along with revised Figs. 10 and 13, showing the changes in red.

With respect to Fig. 10, a drawing correction is being made herewith with respect to the label on the output switch, which should have been S17, not S19. In Fig. 13, reference numeral 152 is being deleted.